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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	51876.P160
First Inventor or Application Identifier	Young-Min Kang
Title	FERROELECTRIC RANDOM ACCESS MEMORY DEVICE CAPABLE OF REDUCING OPERATION FREQUENCY OF REFERENCE CELL
Express Mail Label No.	EM560643880US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. [X] Specification — Total Pages [10]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) (35 CFR 113) — Total Sheets [2]

4. Oath or Declaration — Total Pages [2]
   a. [X] Newly executed (original copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 16 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

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5. [ ] Microfiche Computer Program (*Appendix*)

6. Nucleotide and/or Amino Acid Sequence Submission
(*if applicable, all necessary*)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 CFR 3.73(b) Statement (*when there is an assignee*) [ ] Power of Attorney
9. [ ] English Translation Document (*if applicable*)
10. [X] Information Disclosure Statement (IDS)/PTO - 1449 [X] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [ ] Return Receipt Postcard (MPEP 503)
(*Should be specifically itemized*)
13. [ ] *Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
14. [X] Certified Copy of Priority Document(s)
(*if foreign priority is claimed*)
15. [X] Other: priority request; formal drawings submittal

16. If a **CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ____/____

Prior application Information: Examiner ____ *Group/Art Unit:* ____

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FERROELECTRIC RANDOM ACCESS MEMORY DEVICE CAPABLE OF REDUCING OPERATION FREQUENCEY OF REFERENCE CELL

Field of the Invention

The present invention relates to a semiconductor device; and, more particularly, to a ferroelectric random access memory (FeRAM) device capable of reducing operation frequency of a reference cell.

Description of the Prior Art

Generally, a ferroelectric random access memory (FeRAM) device is a non-volatile semiconductor memory device, which employs the characteristics of a ferroelectric material having the residual polarity of a negative or positive direction. A structure of the ferroelectric random access memory is similar to that of a dynamic random access memory (DRAM) except that a storage element is made of the ferroelectric material.

In the FeRAM, there have been two conventional schemes in order to discriminate whether data written to a memory cell is "0" or "1". The first conventional scheme employs a plurality of memory cells arranged in a matrix, each of which includes two transistors and two ferroelectric capacitors. The data discrimination of the first conventional scheme is accomplished by using the two ferroelectric capacitors, which are connected to a pair of bit lines, e.g. a bit line and a bit line bar, wherein one ferroelectric capacitor is connected to the bit line and the other ferroelectric

capacitor is connected to the bit line bar. That is, a "1" is written to one ferroelectric capacitor and a "0" is written to the other ferroelectric capacitor.

On the other hand, a second conventional scheme employs a plurality of memory cells arranged in a matrix, each of which includes one transistor and one ferroelectric capacitor, while one column of the memory cells is provided with one reference cell having a storage element, i.e. a ferroelectric capacitor. To discriminate whether data written to a memory cell is "0" or "1", the reference cell has the average of electric charges applied to a bit line. Accordingly, the data discrimination of the second conventional scheme is accomplished by using the reference cell, which discharges the average electric charges.

The second conventional scheme may reduce a cell area more than the first conventional scheme. However, every time each memory cell contained in the same column is selected, the corresponding reference cells should be also selected. Therefore, since operation frequency of the reference cell is greater than that of each memory cell contained in the same column, the ferroelectric capacitors of the corresponding reference cell are fatigued faster than the ferroelectric capacitor of each memory cell contained in the same column. As a result, the life span of the ferroelectric capacitor of the reference cell can be severely reduced, thereby affecting the reliance of the FeRAM.

Summary of the Invention

It is, therefore, an object of the present invention to provide a ferroelectric random access memory (FeRAM) that reduces operation frequency of a reference cell, thereby reducing the fatigue of a ferroelectric capacitor of the reference cell.

In accordance with an aspect of the present invention, there is provided a ferroelectric random access memory (FeRAM) device, comprising: a plurality of memory cells arranged in an M × J matrix, wherein M is a positive integer more than three and J is a positive integer; a number of reference cells connected to each column of the memory cells; and a cell selection means for selecting a memory cell in response to address signals from an external circuit and selecting a reference cell corresponding to the selected memory cell.

Brief Description of the Drawings

Other objects and aspects of the invention will become apparent from the following description of the embodiments with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram showing memory cells and reference cells of a ferroelectric random access memory device in accordance with the present invention; and

Fig. 2 is a circuit diagram showing a memory cell selection circuit and a reference cell selection circuit connected to Fig. 1.

Detailed Description of the Invention

Referring to Fig. 1, a ferroelectric random access memory (FeRAM) device in accordance with the present invention includes a plurality of memory cells 10 connected to a bit line BL0 and a number of reference cells 20 connected to a bit line BL1 adjacent to the bit line BL0. The memory cells 10 is arranged in an M × J matrix, wherein M is a positive integer more than three and J is a positive integer. If the number of memory cells of each column is $M = 2^N$, the number of reference cells is N. For example, if the number of the memory cells is 2^8, the number of the reference cells is eight. The N number of reference cells 20 connected to each column of the memory cells 10. For the sake of convenience, an M × 1 matrix of memory cells is shown in Fig. 1.

Also, a cell plate CP0 is positioned between the bit line BL0 and the bit line BL1. The memory cells 10, each of which includes one transistor and one ferroelectric capacitor. Similarly, the reference cells 20, each of which includes one transistor and one ferroelectric capacitor. When one of word lines (WL0 to WLM-1) is selected to operate one of the memory cells 10, a ferroelectric capacitor of the memory cell 10 operated discharges electric charges to the bit line BL0. When one of reference word lines (RWL0 to RWLN-1) is selected to operate one of reference cells 20, a ferroelectric capacitor of the reference cell 20 operated discharges electric charges to the bit line BL1.

Accordingly, the data discrimination is accomplished by

comparing the electric charges of the reference cell 20 with that of the memory cell 10. At this time, the operation frequency of the reference cells 20 is reduced more than that of the conventional reference cell. Thus, the reduction of the magnitude of residual polarity can be delayed in the ferroelectric capacitor of the reference cells 20 and its life span can be increased.

Referring to Fig. 2, the memory cells 10 shown in Fig. 1 are connected to a memory cell selection circuit 200 and the reference cells 20 shown in Fig. 1 are connected to a reference cell selection circuit 300.

The memory cell selection circuit 200 includes NAND gates 201 and inverters 202 to generate a memory cell selection signal in response to address signals. Also, the reference cell selection circuit 300 includes NAND gates 301 and inverters 302 to generate a reference cell selection signal to select a corresponding reference cell.

When it is assumed that the memory cell selection circuit 200 is connected to the memory cells 10 via 256 word lines WL0 to WL255, a NAND gate 201 receives eight address signals from an external circuit. The NAND gate 201 performs NAND logical operation, and an inverter 202 inverts an output signal of the NAND gate 201 to generate the memory cell selection signal, wherein the NAND gate 201 has eight input terminals.

The reference cell selection circuit 300 includes NAND gates 301 and inverters 302 to generate a reference cell selection signal. When it is assumed that the reference cell selection circuit 300 is connected to the reference cells via eight reference word lines

RWL0 to RWL7, a NAND gate 301 receives three address signals from the external circuit. The NAND gate 301 performs NAND logical operation and an inverter 302 inverts an output signal of the NAND gate 301 to generate the reference cell selection signal, wherein the NAND gate 301 has three input terminals.

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

What is claimed is:

1. A ferroelectric random access memory (FeRAM) device, comprising:

a plurality of memory cells arranged in an M × J matrix, wherein M is a positive integer more than three and J is a positive integer;

a number of reference cells connected to each column of the memory cells; and

a cell selection means for selecting a memory cell in response to address signals from an external circuit and selecting a reference cell corresponding to the selected memory cell.

2. The FeRAM device as recited in claim 1, wherein the number of memory cells of each column is $M = 2^N$ and the number of reference cells is N.

3. The FeRAM device as recited in claim 1, wherein said cell selection means includes:

a memory cell selection circuit connected to the memory cells via word lines for generating a memory cell selection signal in response to the address signals to select a corresponding memory cell; and

a reference cell selection circuit connected to the reference cells via reference word lines for generating a reference cell selection signal to select the corresponding reference cell.

4. The FeRAM device as recited in claim 3, wherein said memory

cell selection circuit includes:

a plurality of NAND gates, each NAND gate for receiving address signals from an external circuit to perform NAND logical operation; and

a plurality of inverters, each inverter for inverting an output signal of each NAND gate to generate the memory cell selection signal.

5. The FeRAM device as recited in claim 3, wherein said reference cell selection circuit includes:

a plurality of NAND gates, each NAND gate for receiving address signals from an external circuit to perform NAND logical operation; and

a plurality of inverters, each inverter for inverting an output signal of each NAND gate to generate the reference cell selection signal.

6. The FeRAM device as recited in claim 1, wherein the number of the memory cells is 2^8 and the number of the reference cells is eight.

7. The FeRAM device as recited in claim 4, wherein each NAND gate of said memory cell selection circuit has eight input terminals.

8. The FeRAM device as recited in claim 5, wherein each NAND gate of said reference cell selection circuit has three input

terminals.

9. The FeRAM device as recited in claim 1, wherein said memory cells have one transistor and one ferroelectric capacitor, respectively.

10. The FeRAM device as recited in claim 1, wherein said reference cells have one transistor and one ferroelectric capacitor, respectively.

11. The FeRAM device as recited in claim 1, wherein said memory cells are connected to first bit line.

12. The FeRAM device as recited in claim 11, wherein said reference cells are connected to second bit line.

13. The FeRAM device as recited in claim 12, wherein said memory cells and said reference cells shares a cell plate, wherein the cell plate is positioned between the first bit line and the second bit line.

Abstract of the disclosure

A ferroelectric random access memory (FeRAM) device, includes: a plurality of memory cells arranged in an M × J matrix, wherein M is a positive integer more than three and J is a positive integer; a number of reference cells connected to each column of the memory cells; and a cell selection means for selecting a memory cell in response to address signals from an external circuit and selecting a reference cell corresponding to the selected memory cell.

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Express Mail #: EM560643880US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the application of:

Young-Min Kang

For: FERROELECTRIC RANDOM ACCESS MEMORY DEVICE CAPABLE OF REDUCING OPERATION FREQUENCY OF REFERENCE CELL

SUBMISSION OF FORMAL DRAWINGS

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Submitted herewith are Figures 1-2 in connection with the above-identified application.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 10/27/99

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FIG. 1

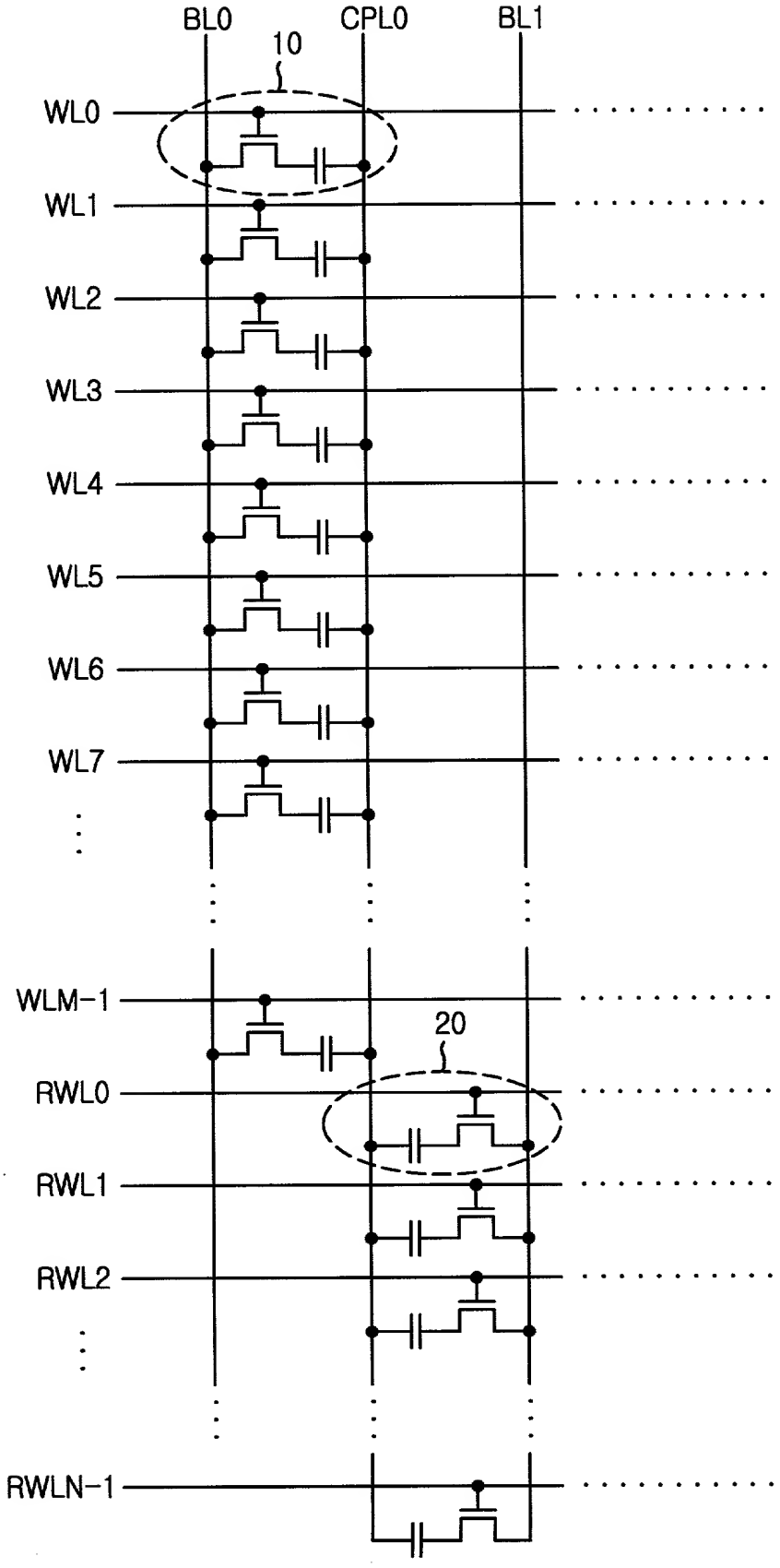
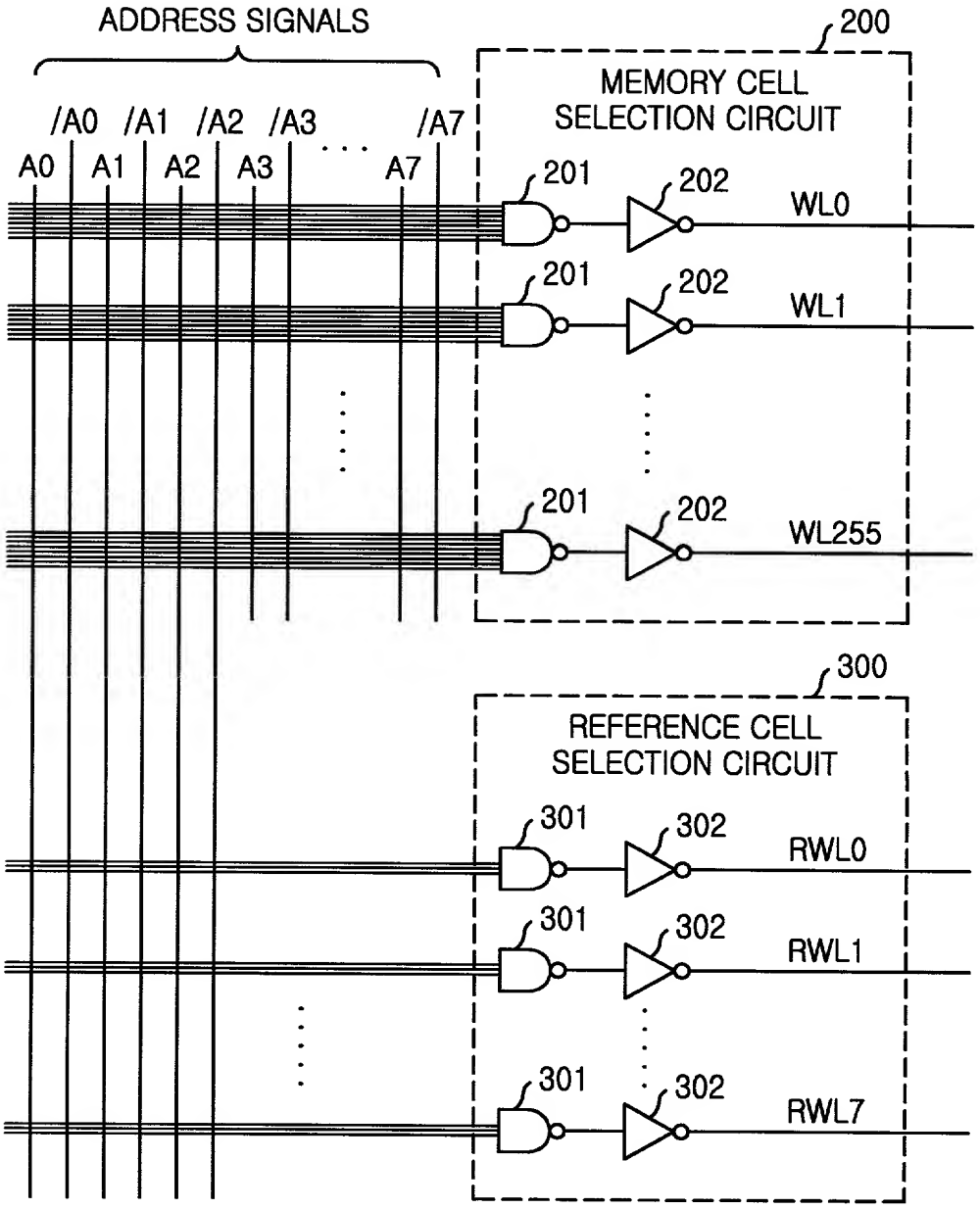

BL0
CPL0
BL1
10
WL0
WL1
WL2
WL3
WL4
WL5
WL6
WL7
WLM-1
20
RWL0
RWL1
RWL2
RWLN-1

FIG. 2


ADDRESS SIGNALS
200
MEMORY CELL SELECTION CIRCUIT
/A0
/A1
/A2
/A3
/A7
A0
A1
A2
A3
A7
201
202
WL0
WL1
WL255
300
REFERENCE CELL SELECTION CIRCUIT
301
302
RWL0
RWL1
RWL7

Our Ref.: 51876.P160

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first an joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled FERROELECTRIC RANDOM ACCESS MEMORY DEVICE CAPABLE OF REDUCING OPERATION FREQUENCY OF REFERENCE CELL

the specification of which

x is attached hereto.

____ was filed on ________________ as

Application Serial No. ________________

and was amended on ________________

(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I do not know and do not believe that the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, ant that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35,, United States Code, Section 119, of ay foreign application(s) for patent or invertor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed: Yes	No
1998-45301	REPUBLIC OF KOREA	28 / 10 / 1998	X	

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, a firm including: Bradley J. Bereznak, revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor KANG, YOUNG-MIN

Inventor's Signature ______ Date 1/9/1999

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Full Name of Second/Joint Inventor ______

Inventor's Signature ______ Date ______

Residence ______ (City, State) Citizenship ______ (Country)

Post Office Address ______

Full Name of Third/Joint Inventor ______

Inventor's Signature ______ Date ______

Residence ______ (City, State) Citizenship ______ (Country)

Post Office Address ______

Full Name of Fourth/Joint Inventor ______

Inventor's Signature ______ Date ______

Residence ______ (City, State) Citizenship ______ (Country)

Post Office Address ______

Full Name of Fifth/Joint Inventor ______

Inventor's Signature ______ Date ______

Residence ______ (City, State) Citizenship ______ (Country)

Post Office Address ______